

**WHAT IS CLAIMED IS:**

1. A method of manufacturing a microelectronic device, comprising:  
performing a first inspection of a device feature during an intermediate stage of manufacture;  
cleaning the device feature after the first inspection; and  
performing a second inspection of the device feature after cleaning the device feature.
2. The method of claim 1 wherein the first inspection is performed by a first inspection tool and the second inspection is performed by a second inspection tool different than the first inspection tool.
3. The method of claim 1 wherein the first and second inspections are performed by a single inspection tool.
4. The method of claim 1 wherein at least one of the first and second inspections is performed by a scanning electron microscope (SEM).
5. The method of claim 1 wherein the cleaning comprises exposing the device feature to an oxygen containing plasma.
6. The method of claim 1 wherein the device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer.
7. The method of claim 1 wherein the device feature is located in a production region of a wafer, the wafer further including a calibration region having a calibration feature located therein.

8. The method of claim 7 wherein the calibration feature comprises a first conductive layer located over the wafer, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer.

9. The method of claim 8 wherein the first conductive layer comprises AlCu, the second conductive layer comprises W, and the buffer layer comprises:

a first TiN layer over the first conductive layer;  
an implanted Ti layer over the first TiN layer; and  
a second TiN layer over the implanted Ti layer.

10. A method of calibrating a metrology tool, comprising:  
inspecting a calibration feature;  
cleaning the inspected calibration feature;  
re-inspecting the cleaned calibration feature; and  
comparing results obtained during the inspection and re-inspection of the calibration feature.

11. The method of claim 10 wherein the initial inspection of the calibration feature is performed by a first metrology tool and the re-inspection of the cleaned calibration feature is performed by a second metrology tool.

12. The method of claim 11 wherein at least one of the first and second metrology tools comprises a scanning electron microscope (SEM).

13. The method of claim 10 wherein the calibration feature comprises an AlCu layer located over a wafer, a first TiN layer located over the AlCu layer, an implanted Ti layer located over the first TiN layer, a second TiN layer located over the implanted Ti layer, and a W layer over the second TiN layer.

14. A calibration wafer, comprising:  
a first conductive layer located over a substrate;

a buffer conductive layer located over the first conductive layer;  
a second conductive layer located over the buffer conductive layer; and  
a plurality of trenches extending through the first, buffer, and second conductive layers,  
thereby defining a plurality of calibration features.

15. The calibration wafer of claim 14 wherein the buffer conductive layer is located on the first conductive layer and the second conductive layer is located on the buffer conductive layer.

16. The calibration wafer of claim 14 wherein the first conductive layer comprises AlCu, the second conductive layer comprises W, and the buffer conductive layer comprises:  
a first TiN layer;  
an implanted Ti layer located over the first TiN layer; and  
a second TiN layer located over the implanted Ti layer.

17. A method of manufacturing a calibration wafer, comprising:  
forming a first conductive layer over a substrate;  
forming a buffer conductive layer over the first conductive layer;  
forming a second conductive layer over the buffer conductive layer; and  
forming a plurality of trenches extending through the first, buffer, and second conductive layers, thereby defining a plurality of calibration features.

18. The method of claim 17 wherein forming the plurality of trenches employs focused ion beam (FIB) milling.

19. The method of claim 17 wherein the focused ion beam comprises Ga.

20. The method of claim 17 wherein forming the buffer conductive layer comprises:  
forming a first TiN layer over the first conductive layer;  
forming an implanted Ti layer over the first TiN layer; and

forming a second TiN layer employing chemical-vapor-deposition over the implanted Ti layer.

21. A microelectronic device, comprising:
- at least one integrated circuit device located in a production region of a wafer, the integrated circuit device including:
- a plurality of semiconductor devices located over the wafer;
  - a plurality of interconnects located over and interconnecting ones of the plurality of semiconductor devices; and
- at least one calibration feature located in a calibration region of the wafer, the calibration feature including:
- a first conductive layer located over the substrate;
  - a buffer conductive layer located over the first conductive layer;
  - a second conductive layer located over the buffer conductive layer; and
  - a plurality of trenches extending through the first, buffer, and second conductive layers, thereby defining the at least one calibration feature.

22. The microelectronic device of claim 21 wherein the first conductive layer comprises AlCu, the second conductive layer comprises W, and the buffer conductive layer comprises:
- a first TiN layer;
  - an implanted Ti layer located over the first TiN layer; and
  - a second TiN layer located over the implanted Ti layer.